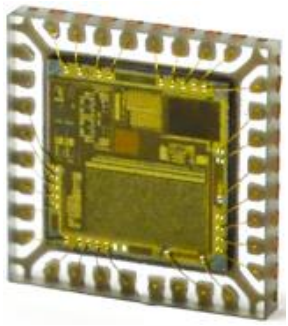
FlexSense® I-Series Programmable Incremental Encoder

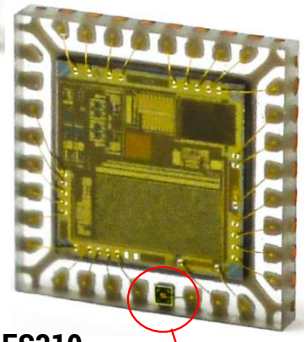
FS210/FS310 Datasheet

Description:

The FS210/FS310 contains a revolutionary optical sensor array that can be programmed to operate with a wide range of code-wheel diameters, including linear strips, and resolutions. This programmable sensor is packaged standalone in a compact Opto-QFN package for the FS210, and a near-IR LED is combined with the sensor in the same package for the FS310. With unparalleled flexibility and versatility in a robust, subcompact package, with closed-loop LED driver control, with on-chip interpolation, and with support for automated alignment and configuration, the FlexSense™ products redefine flexibility.



FS210



FS310

Near-IR LED Chip

How we help you:

- Accelerate time-to-market by reducing engineering cost and effort
- Reduce portfolio complexity with a “one-size-fits-many” solution
- Increase manufacturing throughput and cost efficiency
- Promote product innovation

Features and Benefits:

- Incremental optical encoder sensor IC in 32-pin 5mm x 5mm x 0.65mm OQFN package
- Both transmissive (FS210) and reflective (FS310) variants available.
- User-programmable, high-resolution photosensor pixel array enables quick customization and improves time-to-market.
    - Customizable quadrature- and index-track dimensions
    - Analog or digital quadrature-track output
- Compatible with code-wheel resolution of up to 1,200 lines per inch, or 4,096 PPR at a 15mm optical radius
- Programmable auto-configuration simplifies assembly and alignment.
- Closed-loop LED drive control
- IR LED embedded in the same package (FS310 only)
- Diagnostic functionality:
    - High-temperature fault (with interrupt signaling feedback)
    - LED-drive control loop out of regulation (with interrupt signaling feedback)
    - Power-on reset (with interrupt signaling feedback)
    - Code-wheel eccentricity
- I^2C interface
- -40°C to +125°C ambient operating temperature
- On-chip quad-track interpolation (2x, 4x, 8x) and division (by powers of 2 up to 2,048)
- Quad-track output characteristics at native frequency up to 400kHz:
    - THD ≤ 1.0% on analog outputs
    - Transient noise ≤ 1.0% of signal amplitude on analog outputs at 40mW/cm2 input power density
    - Angular position accuracy ±1 part in 100K, or about 12 arc-seconds at 1,500 PPR, on digital outputs
- Single-supply (3.3V ± 10%) operation

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FS210/FS310 Datasheet

General Description

The FS210/FS310 is a user-configurable single-chip solution for an incremental optical encoder, available in a surface-mount high-usage-temperature-tolerant package. The sensor is available for both transmissive (FS210) and reflective (FS310) applications. Its programmable photosensor pattern can accommodate code wheels with printing densities of up to 1,200 lines per inch, which corresponds to more than 4,096 pulses per revolution (PPR) at an optical radius of 15mm. It provides complementary quadrature– and index-track outputs. Its quadrature outputs are configurable as either analog (with ≤ 1% THD, enabling high-quality off-chip interpolation) or digital (with low quadrature error) with up to 8x interpolation or programmable down-division by up to 2,048x in order to handle a wider logical PPR range. Its digital index-track output can be configured to be synchronized to either quadrature output, for a pulse width of exactly one-half cycle, or to both quadrature outputs, for a pulse width of exactly one-quarter cycle. The FS310 includes an in-package LED, and both the FS210/FS310 include an integrated driver that is user-configurable either to drive a fixed user-configurable current or as part of a closed-loop control system to produce a fixed optical input power density over its photosensors. The easy-to-use I^2C interface and memory-mapped photosensor configuration enable automated alignment and signal conditioning during encoder module assembly, all from a single 3.3V ±10% supply.

Package Pinout

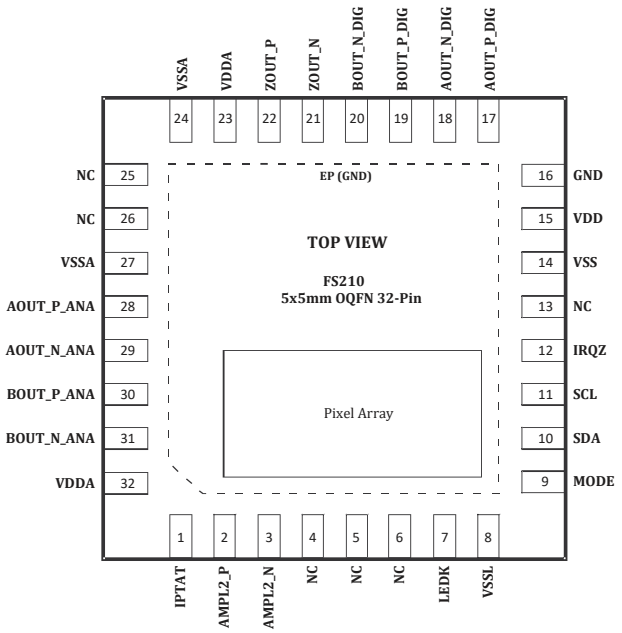

Figure 1: FS210 Pin Configuration (5mm x 5mm OQFN - top view)

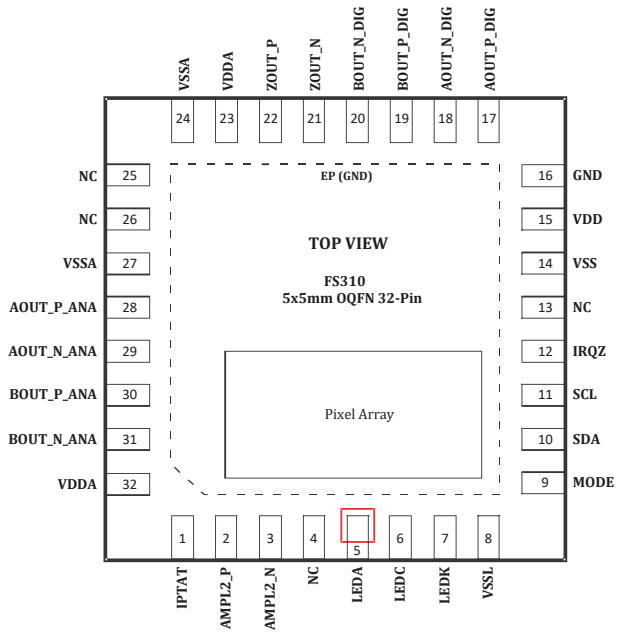

Figure 2: FS310 Pin Configuration (5mm x 5mm OQFN - top view)

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Pin Descriptions

Table 1: Pin Description

Pin Number	Pin Name	Description
1	IPTAT	Analog temperature-sense current output: **[0x88D] bits <5:4> = 11b**: Current sunk (into the pin) is proportional to absolute temperature. **[0x88D] bits <5:4> = 00b**: Output is floating.
2, 3	AMPL2_P, AMPL2_N	Analog amplitude-check voltage differential output: **[0x88D] bits <5:4> = 11b**: Difference of two pin voltages is the sum of the squares of the A and B quadrature amplitudes. **[0x88D] bits <5:4> = 00b**: Outputs are floating.
4, 13, 25, 26	DNC	DO NOT CONNECT
5	DNC/LEDA	LED anode (must connect off-chip to VDDA), **FS310 only**
6	DNC/LEDC	LED cathode (must connect to LEDK), **FS310 only**
7	LEDK	LED drive current source (must connect to LEDC on FS310)
8	VSSL	Ground return for LED drive current
9	MODE	Digital input to select between I^2C master or slave setting at power-up: **Logic-0**: Slave mode selected **Logic-1:** Master mode selected
10	SDA	Open-drain I^2C data
11	SCL	Open-drain I^2C clock
12	IRQZ	Open-drain system interrupt output
14, 16	VSS	Digital ground connection (must connect to both at board level)
15	VDD	Digital positive voltage supply
17	AOUT_P_DIG	Digital quadrature-track positive-sense A (cosine) output
18	AOUT_N_DIG	Digital quadrature-track negative-sense A (cosine) output
19	BOUT_P_DIG	Digital quadrature-track positive-sense B (sine) output
20	BOUT_N_DIG	Digital quadrature-track negative-sense B (sine) output
21	ZOUT_N	Digital negative-sense index-track output
22	ZOUT_P	Digital positive-sense Index track output
23	VDDA	Analog positive voltage supply
24, 27	VSSA	Analog ground connection (must connect to both at board level)
28	AOUT_P_ANA	Analog quadrature-track positive-sense A (cosine) output
29	AOUT_N_ANA	Analog quadrature-track negative-sense A (cosine) output
30	BOUT_P_ANA	Analog quadrature-track positive-sense B (sine) output
31	BOUT_N_ANA	Analog quadrature-track negative-sense B (sine) output
32	VDDA	Analog positive voltage supply
EP_GND	VSS	Exposed backside thermal pad (must connect to pins 14, 16 at board level)

Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings[1]

Characteristic	Min	Max	Unit
Storage Temperature	-55	135	°C
Operating Temperature	-40	125	°C
Potential difference between any two pins of the same net (VSS, VSSA, LEDK)	-0.05	0.05	V
Potential difference between VDD and VDDA pins	-0.5	0.5	V
Potential difference between any two of VSS, VSSA, and VSSL	-0.05	0.05	V
Potential on (VDD, VDDA or LEDA) pin with respect to (VSS, VSSA, or VSSL) pin	-0.5	5.0	V
Potential on any other pin with respect to VSS, VSSA, or VSSL pin	-0.5	5.0	V
Potential on any other pin with respect to VDD or VDDA pin	-5.0	0.5	V
Current into/out of VDD, VDDA, VSS, or VSSA pin	-50	50	mA
Current into/out of LEDA, LEDK, or VSSL pin	-100	100	mA
Current into/out of any analog quadrature-track output pin (AOUT_P_ANA, AOUT_N_ANA, BOUT_P_ANA, or BOUT_N_ANA)	-5	5	mA
Current into/out of any other pin	-25	25	mA
Incident optical power density		50	mW/cm^2
Reflow temperature, MSL-6 (5 seconds or less at this temperature; 40 seconds or less within 5°C of this temperature)		260	°C
Electrostatic discharge immunity (HBM)	±4		kV

[1] Functional and testing operating conditions given in Table 3. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Prolonged operation of the device at these conditions may result in permanent damage to the device.

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Electrical/Optical Characteristics

Table 3. Electrical and Optical Operating Characteristics.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit	Notes
GENERAL CHARACTERISTICS							
Ambient temperature	T_A		-40	-	125	°C	1
Thermal shutdown trip point	T_{jSL}		135	150	170	°C	2
Thermal alarm trip point	T_{jAL}	X = TALM<3:0>	195-9.5X	200-9X	205-8.5X	°C	3
Supply voltage	V_{DD}, V_{DDA}		2.97	3.30	3.60	V	4
Supply voltage power-up time	t_{PU}	From 0.1V to (V_{DDA}, V_{DD} – 0.1V)	100			us	
Wake-up time	t_{WU}	MODE = 0		2.5		ms	
		MODE = 1		95.5		ms	
Active current (analog)	I_{DDA}	QCFG=0x00; f=1kHz		9.0	12.0	mA	4, 5
Active current (digital)	I_{DD}	QCFG=0x13; f=1kHz		2.0		mA	4, 5
PHOTODIODES							
Wavelength of incident power	λ		400		950	nm	
QUADRATURE-TRACK DIGITAL CHARACTERISTICS							
Output high current	$I_{OH:QD}$	QCFG<4> = 1; V_{OH} = V_{DD} - 0.4V		-15		mA	6
Output low current	$I_{OL:QD}$	QCFG<4> = 1; V_{OL} = 0.4V		28		mA	
Output high short-circuit current limit	$I_{OHL:QD}$	QCFG<4> = 1; Pin shorted to VSS		-50		mA	6
Output low short-circuit current limit	$I_{OLL:QD}$	QCFG<4> = 1; Pin shorted to V_{DD}		90		mA	
Output extrinsic fall time	$t_{F:Q}$	QCFG<4>=1; C_L=20pF; 90% to 10% of V_{DD}		10		ns	
Output extrinsic rise time	$t_{R:Q}$	QCFG<4>=1; C_L=20pF; 10% to 90% of V_{DD}		10		ns	
Digital phase error	ε_ϕ	1σ; f≤100kHz; QCFG=0x10 (1x interpolation)		0.4		°	5, 7, 8, 9
		1σ; f≤100kHz; QCFG=0x13 (8x interpolation)		7.5			
Duty cycle variation	ΔD_Q	1σ; f≤100kHz; QCFG=0x10 (1x interpolation)		0.2		%	5, 8, 9
		1σ; f≤100kHz; QCFG=0x13 (8x interpolation)		2		%	
Period jitter	$\Delta\tau_P/\tau$	1σ; f≤100kHz; QCFG=0x10 (1x interpolation)		0.2		%	5, 8, 9
		1σ; f≤100kHz; QCFG=0x13 (8x interpolation)		2		%	
Cycle-to-cycle jitter	$\Delta\tau_{CC}/\tau$	1σ; f≤100kHz; QCFG=0x10 (1x interpolation)		0.3		%	5, 8, 9
		1σ; f≤100kHz; QCFG=0x13 (8x interpolation)		3		%	

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Characteristic	Symbol	Conditions	Min	Typ	Max	Unit	Notes
QUADRATURE-TRACK ANALOG CHARACTERISTICS							
Output high short-circuit current limit	$I_{OHL:QA}$	QCFG<4> = 0; Pin shorted to VSS		-1.2		mA	
Output low short-circuit current limit	$I_{OLL:QA}$	QCFG<4> = 0; Pin shorted to V_{DD}		2.5		mA	
Equivalent transimpedance gain	$Z_{Q:LN}$	TQM2=0x00; ZCFG<6> = 1 (low noise)		2.9		MΩ	5, 8
Input Frequency		TQM2=0x00; ZCFG<6> = 1 (low noise)			400	kHz	5, 8
Output common-mode voltage	$V_{O:Q}$	QCFG=0x00		1.25		V	5, 8
Output noise voltage	$\lvert V_{N:LN} \rvert$	ZCFG<6> = 1; integrated over f ≤ 300kHz		2		mV	5, 8
	$\lvert V_{N:HS} \rvert$	ZCFG<6> = 1; integrated over f ≤ 3MHz		20		mV	
Total harmonic distortion	THD_Q	f≤100KHz		-40		dB	5, 8
INDEX TRACK CHARACTERISTICS							
Output high current	$I_{OH:Z}$	$V_{OH} = V_{DD} – 0.4V$		-15		mA	6
Output low current	$I_{OL:Z}$	$V_{OL} = 0.4V$		28		mA	
Output high short-circuit current limit	$I_{OHL:Z}$	Pin shorted to VSS		-50		mA	6
Output low short-circuit current limit	$I_{OLL:Z}$	Pin shorted to V_{DD}		90		mA	
Output extrinsic fall time	$t_{F:Z}$	C_L = 20pF; From 90% to 10% of V_{DD}		10		ns	
Output extrinsic rise time	$t_{R:Z}$	C_L = 20pF; From 10% to 90% of V_{DD}		10		ns	
LED DRIVER CHARACTERISTICS							
LEDK pin voltage	V_K	T_A ≤ -40°C; $I_{OL:K}$ ≤ 85mA	0.60			V	
		T_A ≤ 25°C; $I_{OL:K}$ ≤ 85mA	0.70				
		T_A ≤ 125°C; $I_{OL:K}$ ≤ 85mA	0.80				
LEDK output current	$I_{OL:K}$	ILED = 0x00; $V_{K(min)} \le V(LEDK) \le V_{K(max)}$		0.1	10.0	µA	10
		ILED = 0x01; $V_{K(min)} \le V(LEDK) \le V_{K(max)}$		0.60		mA	
		ILED = 0x7F; $V_{K(min)} \le V(LEDK) \le V_{K(max)}$		80		mA	
LEDK current differential non-linearity	$DNL_{I:K}$	ILED<7> = 0; $V_{K(min)} \le V(LEDK) \le V_{K(max)}$	-0.75		0.75	LSB	11
Closed-loop LED current update period	$t_{upd:N}$	LEDLP<7> = 0; ILED<7> = 1		16		s	
LED drive-alarm threshold	$I_{OLA:K}$		0.875*ILED<6:0>			mA	
MODE PIN CHARACTERISTICS							
Input low voltage	$V_{IL:M}$				0.3*V_{DD}	V	

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Characteristic	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH:M}$		0.7*V_{DD}			V	
Input leakage current	$I_{L:M}$	0V ≤ V(pin) ≤ V_{DD}, at 25°C	-0.1		0.1	µA	
PREVENTIVE MAINENANCE OUTPUT CHARACTERISTICS							
Proportional-to-absolute-temperature output current	I_{PTAT}	T_j = 25°C		10.4		µA	
		T_j = 125°C		14.8		µA	
Wobble-detect coefficient	k_W			4		µA/V^2	
I²C PIN CHARACTERISTICS							
Input low voltage	V_{IL}				0.3*V_{DD}	V	
Input high voltage	V_{IH}		0.7*V_{DD}			V	
Output low current	I_{OL}	V_{OL} = 0.4V	3			mA	
Output fall time	t_{OF}	From $V_{IH(min)}$ to $V_{IL(max)}$			250	ns	
Input capacitance	C_I	Presented by the device only			10	pF	
I²C MASTER/SYSTEM REQUIREMENTS							
SCL low time	t_{LOW}		1.3			µs	
SCL high time	t_{HIGH}		0.6			µs	
START-condition setup time	$t_{SU;STA}$	V_{SCL}↑ → V_{SDA}↓	0.6			µs	
START-condition hold time	$t_{HD;STA}$	V_{SDA}↓ → V_{SCL}↓	0.6			µs	
Data setup time	$t_{SU;DAT}$	V_{SDA}↕ → V_{SCL}↑; for bits being written from the master to this device			100	µs	
Data hold time	$t_{HD;DAT}$	V_{SCL}↓ → V_{SDA}↕; for bits being written from the master to this device	0			µs	
Data valid wait time	$t_{VD;DAT}$	V_{SCL}↓ → V_{SDA} valid; for bits being read from this device by the master			0.9	µs	
STOP-condition setup time	$t_{SU;STO}$	V_{SCL}↑ → V_{SDA}↑	0.6			µs	
Bus free time (between STOP and next START)	t_{BUF}	V_{SDA}↑ → V_{SDA}↓	1.3			µs	
Total capacitance, each of SCL and SDA	C_B	Sum of on-chip (C_I) and off-chip capacitances			400	pF	

1 Thermal self-heating must not increase junction temperature beyond 135°C in normal operation.

2 Tj > TjSL causes output drivers to be disabled, most on-chip static current consumption (LED driver, TIAs, interpolator) to be turned off, and the interrupt status bit INTR<4> to be set to 'b1. Additionally, it causes the IRQZ pin level to be driven to 'b0 if the interrupt mask bit INTR<0> is 'b1. Once the shutdown threshold is tripped, the part remains in shutdown until the user executes an I²C read access to the INTR register or until a power-on reset event occurs.

[3] Tj > TjAL causes the interrupt status bit INTR<5> to be set to 'b1 and the IRQZ pin level to be driven to 'b0 if the interrupt mask bit INTR<1> is 'b1 but does NOT disable output drivers nor turn off on-chip static current consumption. Once the alarm threshold is tripped, the effects persist until the user executes an I^2C read access to the INTR register or until a power-on reset event occurs.

[4] The specified supply current for a particular supply (VDD or VDDA) refers to the sum of the currents sunk by all pins connected to that supply since there are multiple pins for each supply.

[5] Configured to produce 1Vp-p quad-track analog voltages with as close zero differential DC offset as possible; low-noise mode (ZCFG<6> = 1) unless otherwise indicated.

[6] Negative value implies current is flowing out of the pin.

[7] Assuming photocurrents are perfect sinusoids in perfect quadrature - i.e. negligible THD attributable to non-ideality in pixel pattern or mechanical effects.

[8] Deviation from 90° of phase difference between differential A and B analog output voltages or between AOUT_P_DIG and BOUT_P_DIG.

[9] With reference to Figure 3

[10] Measurable only by placing a low-impedance current meter between LEDK and LEDC pins at the package level or by measuring the current into LEDA. Room temperature is assumed for typical conditions and 125°C is assumed for max conditions.

[11] Nominal value of 1 LSB is 0.6mA.

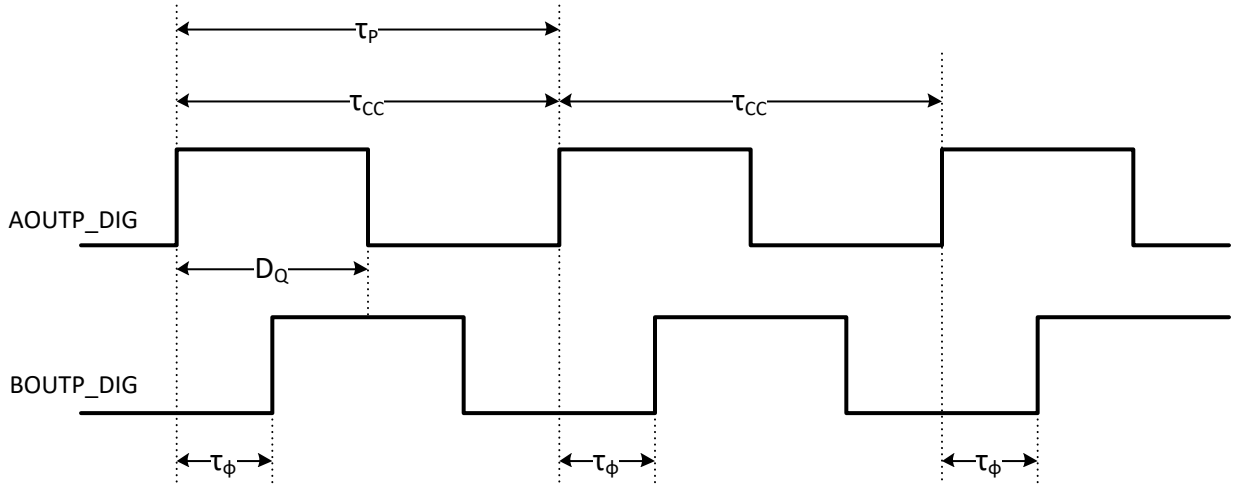

Figure 3: Jitter specification diagram; with τ_P as time period, τ_{CC} as a similar time used to calculate cycle-to-cycle jitter, D_Q as the duty cycle, and τ_Φ as time of the phase difference between A and B. The phase error, ε_Φ, can be calculated as $360(\tau_\Phi/\tau_P)$.

Block Diagram

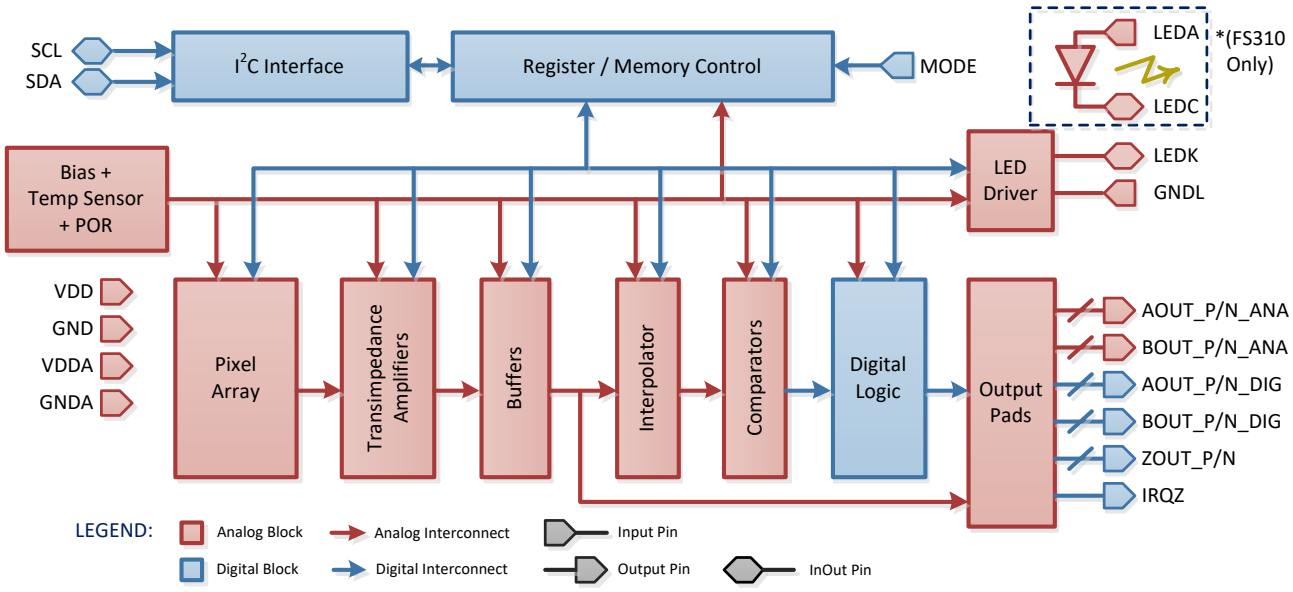

Figure 4: FS210/FS310 Block Diagram

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Memory Mapping

Table 4: FS210/FS310 Memory Map

Address Range	Power-On Reset State	Register	
0x0000 – 0x01FF	<random>	**PXC**	Pixel control bits
0x0200 – 0x03FF	X		<not implemented>
0x0400 – 0x041F	<random>	**CCFG**	Pixel column configuration bits
0x0420 – 0x087F	X		<not implemented>
0x0880	0x00	**TDCA**	Offset trim for A (cosine) quadrature-track signal path
0x0881	0x00	**TDCB**	Offset trim for B (sine) quadrature-track signal path
0x0882	0x00	**TQM1**	Trim to equalize A and B quadrature-track differential output voltage magnitudes
0x0883	0x00	**TQM2**	Trim to change A and B quadrature-track differential buffer gains together
0x0884	0x00	**QCFG**	Quadrature-track output control
0x0885	0x00	**ZCFG**	Index-track output control
0x0886	0x10	**ILED**	LED drive-current open-/closed-loop selection and maximum current magnitude
0x0887	0x26	**LEDLP**	Control bits for closed-loop LED drive control
0x0888	0xCC	**TALM**	Thermal-alarm trip point selection thermal-shutdown/alarm trim
0x0889	0x00	**INTR**	Interrupt mask and status bits
0x088A	0xFF	**TIAE**	Enable bits for quadrature-track and index-track transimpedance amplifiers
0x088B	0x00	**CBFEZ**	Enable bits (active-low) for quadrature-track buffers and quadrature- and index-track comparators
0x088C	0x00	**SIG**	Signature: off-chip NVM should be set up such that master-mode power-up sequence writes 0xAA to this register
0x088D	0x01	**MISC**	Control bits to output PTAT current and $Sin^2x + Cos^2x$ differential currents
0x088E	0x00 or 0xAA	**SIGV**	Signature-verify register (read-only): reads 0x0A if a master-mode power-up sequence completes successfully and 0xAA was copied to SIG during this sequence; reads 0x00 otherwise
0x088F	0x10	**LEDLV**	Actual instantaneous LED drive current (read-only)

Pixel Array Control

Correct operation of the FS210/FS310 requires that its photoactive area, an array of 4,096 pixels (64 rows by 64 columns), be configured to be consistent with the code wheel with which it is being used. Six aggregate photocurrents are produced by the device's photoactive area: the positive- and negative-sense photocurrents for the two quadrature-track outputs and for the index-track output. Each pixel's photocurrent either contributes to one of the six aggregate photocurrents (A+, A-, B+, B-, Z+, Z-) or is shunted to ground, depending on how the pixel is configured.

The on-chip physical dimensions of each pixel are 36.2µm by 18.1µm, so the dimensions of the entire photoactive area are 2.32mm by 1.16mm.

Associated with each pixel is a single SRAM bit called a **Pixel Control (PXC)** bit, and associated with each pixel column are four SRAM bits called a **Column Configuration (CCFG)** nibble. A column's CCFG nibble selects the aggregate photocurrent output to which the active pixels in that column contribute (A+, A-, B+, B-, Z+, Z-, or none). A pixel's PXC bit controls whether that pixel is *active* – i.e. its photocurrent contributes to the aggregate photocurrent output selected by the column's 4-bit control field – or *inactive* – i.e. its photocurrent is shunted to ground.

The 4,096 PXC bits, or 512 bytes, occupy the address range [0x000 – 0x1FF]. The 64 CCFG nibbles, or 32 bytes, occupy the address range [0x400 – 0x41F]. The mapping of logical bytes and bits to physical columns and pixels is detailed below.

The PXC and CCFG bytes are volatile SRAM, so their contents are lost every time the device is power cycled. Therefore, the desired contents must be stored off-chip in non-volatile storage somewhere in the system, and the system must contain a means to copy the patterns from the off-chip non-volatile storage into the on-chip SRAM through the device's I^2C port every time it is powered up. If the system contains a microcontroller with non-volatile storage outside the encoder module, then this microcontroller can contain the non-volatized PXC and CCFG contents. If the system does not contain a microcontroller with non-volatile storage outside the encoder module, then a non-volatile memory chip with an I^2C interface and at least 1Kbyte capacity, such as the M24C32S-FCU from ST, is required.

Table 5: Mapping of PXC and CCFG Registers to Pixel Location

	Col. Grp. 000	Col. Grp. 100	Col. Grp. 001	Col. Grp. 101	Col. Grp. 010	Col. Grp. 110	Col. Grp. 011	Col. Grp. 111
Row 00	[0x0000]	[0x0004]	[0x0001]	[0x0005]	[0x0002]	[0x0006]	[0x0003]	[0x0007]
Row 01	[0x0008]	[0x000C]	[0x0009]	[0x000D]	[0x000A]	[0x000E]	[0x000B]	[0x000F]
Row 02	[0x0010]	[0x0014]	[0x0011]	[0x0015]	[0x0012]	[0x0016]	[0x0013]	[0x0017]
Row 03	[0x0018]	[0x001C]	[0x0019]	[0x001D]	[0x001A]	[0x001E]	[0x001B]	[0x001F]
Rows 04-59	…	…	…	…	…	…	…	…
Row 60	[0x01E0]	[0x01E4]	[0x01E1]	[0x01E5]	[0x01E2]	[0x01E6]	[0x01E3]	[0x01E7]
Row 61	[0x01E8]	[0x01EC]	[0x01E9]	[0x01ED]	[0x01EA]	[0x01EE]	[0x01EB]	[0x01EF]
Row 62	[0x01F0]	[0x01F4]	[0x01F1]	[0x01F5]	[0x01F2]	[0x01F6]	[0x01F3]	[0x01F7]
Row 63	[0x01F8]	[0x01FC]	[0x01F9]	[0x01FD]	[0x01FA]	[0x01FE]	[0x01FB]	[0x01FF]
CCFG	[0x0400 – 0x0403]	[0x0404 – 0x0407]	[0x0408 – 0x040B]	[0x040C – 0x040F]	[0x0410 – 0x0413]	[0x0414 – 0x0417]	[0x0418 – 0x041B]	[0x041C – 0x041F]

Pixel Control Registers (PXC: [0x0000 – 0x01FF])

The mapping of pixels to the PXC bits that control them is as follows: The 64 rows in the pixel array are numbered consecutively, from row 00 at the top to row 63 at the bottom. The 64 columns in the pixel array are divided into eight groups of eight contiguous columns. The column groups are numbered non-consecutively: group 0 contains the leftmost 8 columns, group 4 contains the next-leftmost 8 columns, group 1 contains the next-leftmost 8 columns, then group 5, then group 2, then group 6; group 3 contains the second-rightmost 8 columns, and group 7 contains the rightmost 8 columns. The address of the PXC register that controls a particular set of 8 pixels is found by concatenating the row number (6 bits) and the column group number (3 bits) of the set of pixels, as shown below:

Table 6. PXC Register Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	Row #						Col. Group #		

A single PXC register controls 8 pixels, with the bits from least-significant to most-significant controlling the pixels in the set of 8 from left to right: the least-significant bit controls the leftmost pixel of the 8, and the most-significant bit controls the rightmost pixel of the 8. If the value of the PXC register bit controlling a particular pixel is 1, then the photocurrent of that pixel does contribute to the aggregated output current to which the column is assigned by its CCFG register. If the value of the PXC register bit controlling a particular pixel is 0, then the photocurrent of that pixel is shunted to ground and does not contribute to the aggregated output current to which the column is assigned by its CCFG register.

Table 7. Bits Within a PXC Register

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Rightmost pixel	2nd-rightmost pixel	3rd-rightmost pixel	4th-rightmost pixel	4th-leftmost pixel	3rd-leftmost pixel	2nd-leftmost pixel	Leftmost pixel

Column Configuration Registers (CCFG: [0x0400 – 0x041F])

Each CCFG register controls two adjacent pixel columns: the four least-significant bits control the leftmost of the two columns, and the four most-significant bits control the rightmost of the two columns. The column pairs controlled by individual CCFG registers step from left to right with increasing address: [0x0400] controls the leftmost pair of columns, [0x0401] controls the second-leftmost pair, [0x041E] controls the second-rightmost pair, and [0x041F] controls the rightmost pair. The value of each nibble in a CCFG register selects the aggregated photocurrent (A+, A-, B+, B-, Z+, Z-) to which the photocurrents from all “ON” pixels in the corresponding column contribute, according to the table below.

Table 8. CCFG Byte

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Rightmost column of pair				Leftmost column of pair			

Table 9. CCFG Nibble Mapping

CCFG Nibble	Aggregated Photocurrent
'b0000	A+
'b0001	A-
'b0010	B+
'b0011	B-
'b0100	Z+
'b0101	Z-
All Others	Shunted to Ground

Throughout the remainder of this document, it is assumed that the FlexSense™ is mounted in a rotary encoder system, that its PXC and CCFG registers have been populated to be consistent with the code wheel in that system, and that the code wheel is rotating with constant angular velocity. The direction of rotation is a matter of convention. Given a PXC/CCFG data pattern designed to produce A-leading-B quadrature-track outputs under clockwise code-wheel rotation and B-leading-A outputs under counter-clockwise rotation, it is straightforward to modify the pattern to produce A-leading-B outputs under counter-clockwise rotation and B-leading-A outputs under clockwise rotation. The illustrative figures below assume that the combination of the PXC/CCFG data pattern and the direction of code-wheel rotation produces A-leading-B quadrature-track output signals.

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Quadrature-Track Outputs

Figure 5 below shows the ideal response of the digital quadrature-track output pins (AOUT_P_DIG, AOUT_N_DIG, BOUT_P_DIG, BOUT_N_DIG) to constant-angular-velocity code-wheel rotation, with the FS210/FS310 configured for digital quadrature-track output. Four cases are shown: uninterpolated, 2x interpolation, 4x interpolation, and 8x interpolation. Fully differential outputs are shown in the uninterpolated case, but only the positive-sense signals are shown in the three interpolated cases. Even though they are not shown for all cases in the figure, when the device is configured for differential quadrature-track output, AOUT_N_DIG and BOUT_N_DIG are the logical complements of AOUT_P_DIG and BOUT_P_DIG, respectively, regardless of the configured interpolation factor. When the device is configured for single-ended digital quadrature-track output, then AOUT_N_DIG and BOUT_N_DIG are placed in a high-impedance state. When the device is configured for digital quadrature-track output – either differential or single-ended – then the analog quadrature-track output pins (AOUT_P_ANA, AOUT_N_ANA, BOUT_P_ANA, BOUT_N_ANA) are placed in a high-impedance state. In the Figure 5 and Figure 6, τ_{CW} is the rotational period of the code wheel, and PPR is the number of native pulses per revolution in the code wheel's quadrature track.

Figure 6 below shows the ideal response of the positive-sense digital quadrature-track outputs to constant-angular-velocity code-wheel rotation, with the device configured for digital quadrature-track outputs, for three cases: uninterpolated, divide-by-2, and divide-by-4.

If the FS210/FS310 is configured for analog quadrature-track outputs, then the digital quadrature-track output pins (AOUT_P_DIG, AOUT_N_DIG, BOUT_P_DIG, BOUT_N_DIG) are placed in a high-impedance state, and the analog quadrature-track output (AOUT_P_ANA, AOUT_N_ANA, BOUT_P_ANA, BOUT_N_ANA) waveforms are similar to the aggregated photocurrent waveforms in the figure, centered at $V_{O:Q} \approx 1.25V$ and multiplied by a common effective differential transimpedance.

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Details of quadrature-track output-pin operation are controlled by the QCFG register as shown below:

Quad-Track Configuration Register (QCFG: [0x0884]):

Table 10. QCFG register definition.

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
SE_DZ	NBWL		D_AZ	INTP			

Table 11. QCFG field description.

Bits	Definition
INTP	Digital interpolation or divide-down factor: **0000**: No Interpolation **0001**: 2x multiply **0010**: 4x multiply **0011**: 8x multiply **0100**: Reserved **0101**: x2 divide **0110**: x4 divide **0111**: x8 divide **1000**: x16 divide **1001**: x32 divide **1010**: x64 divide **1011**: x128 divide **1100**: x256 divide **1101**: x512 divide **1110**: x1,024 divide **1111**: x2,048 divide
D_AZ	Analog/digital control for quadrature-track outputs **0**: Analog outputs **1:** Digital outputs
NBWL	**Reserved**: Do not change from power-up default (00)
SE_DZ	Single-ended / differential digital output control. (no effect if D_AZ bit is 0) **0:** Differential (AOUT_P_DIG, BOUT_P_DIG, AOUT_N_DIG, BOUT_N_DIG all driven when D_AZ = 1) **1:** Single-ended (AOUT_P_DIG and BOUT_P_DIG driven; AOUT_N_DIG and BOUT_N_DIG not driven when D_AZ = 1)

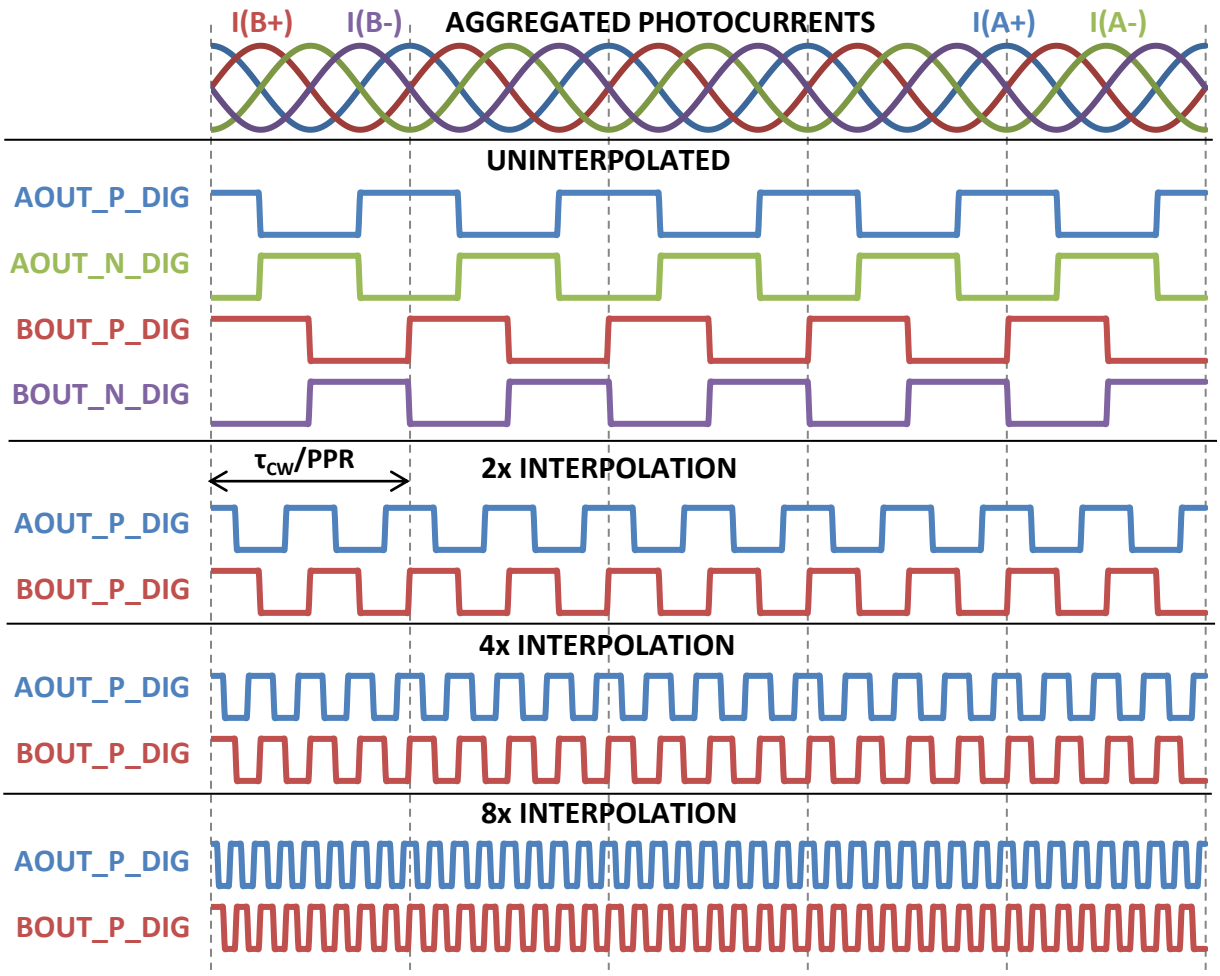

Figure 5: Quad-track outputs (Clockwise rotation; analog, digital 1x – 8x interpolation)

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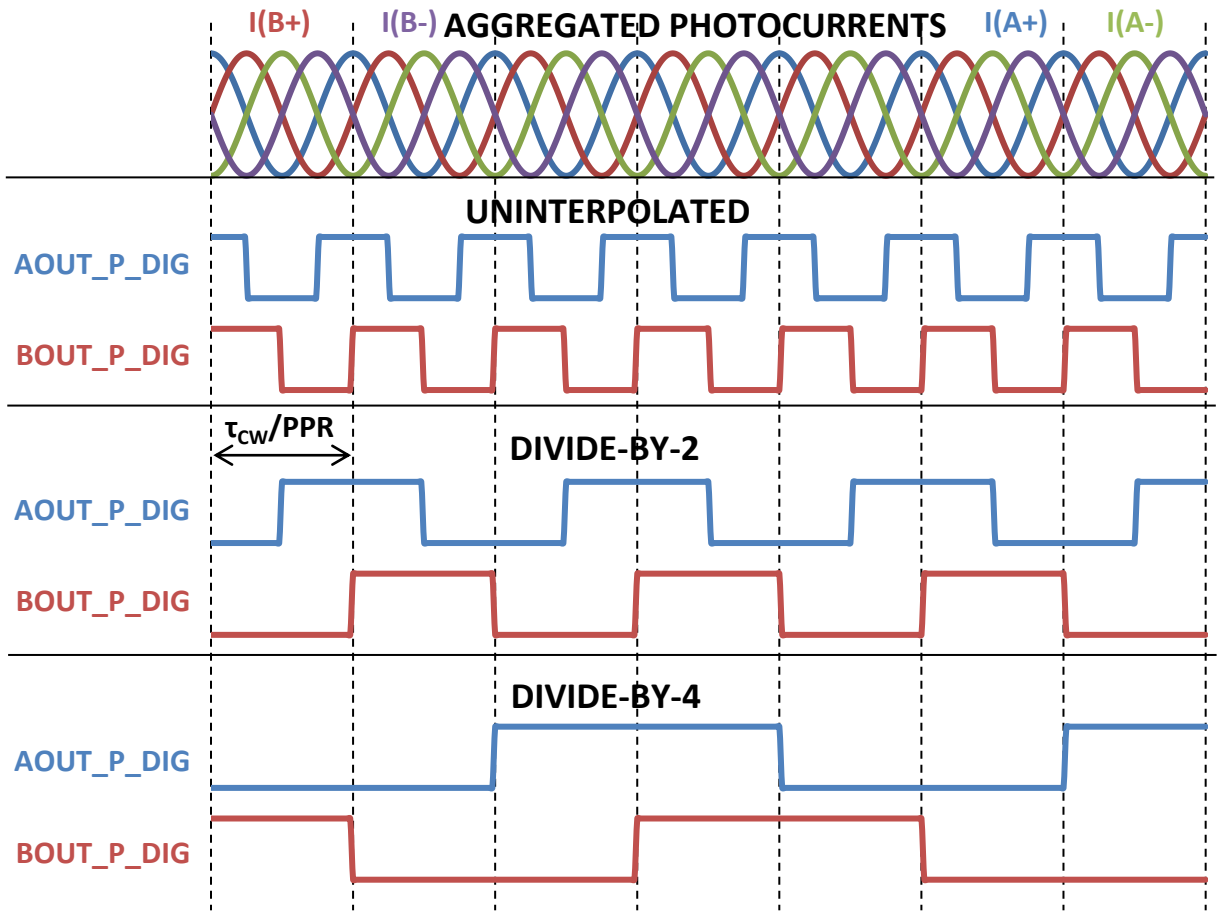

Figure 6: Quad-track outputs (Clockwise rotation; analog, digital uninterpolated, divide-by-2, -4)

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Index-Track Outputs

The digital index-track outputs ZOUT_P and ZOUT_N are intended to produce one single pulse per code-wheel revolution, provided the code wheel is designed properly for that purpose and the PXC/CCFG data pattern is consistent with the code wheel. ZOUT_P is intended to be low for most of the code-wheel revolution and to have a single high-going pulse once per revolution. ZOUT_N is the logical complement of ZOUT_P and therefore is intended to be high for most of the code-wheel revolution and to have a single low-going pulse once per revolution, coincident with the single high-going pulse on ZOUT_P.

The Index-Track Configuration Register ZCFG controls whether the index-track output is differential – i.e. both ZOUT_P and ZOUT_N to complementary logic levels – or single-ended – i.e. the FS210/FS310 places ZOUT_N in a high-impedance state and only drives ZOUT_P. ZCFG also controls the timing of the single pulse on ZOUT_P/ZOUT_N with respect to the quadrature-track outputs.

Additionally, ZCFG contains a bit that affects the quadrature-track signal path: The power-on default state (0) of the TLNM bit allows for analog quadrature-track signal frequencies as high as 1MHz, but with comparatively low transimpedance, so a comparatively higher buffer gain is required in order to achieve adequate signal amplitude, which also gains noise and therefore degrades signal quality. In low-noise mode (TLNM = 1), the quadrature-track transimpedance is comparatively higher, so less buffer gain is needed, producing less output-referred noise and better signal quality, but at the cost of limiting the analog quadrature-track signal frequency to no more than 400kHz.

Index Track Gating

The ZOUT signals can optionally be gated by the quadrature outputs as detailed in the section below. All the gating features are defined with $Z_+ - Z_-$ tracks are greater than 0 and $X_+ - X_-$ is less than 0, where X is either A or B as chosen in the ZCFG register. If the opposite polarity of the quadrature signal is desired, i.e. $X_+ - X_-$ is greater than 0, please contact the factory.

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Index-Track Configuration Register (ZCFG: [0x0885]):

Table 12. ZCFG register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD	TLNM (‘b1)	RSVD		SE_DZ	RSVD	ZGCTL	

Table 13. ZCFG field description

Bits	Description
ZGCTL	Index-pulse gating control: **00**: Ungated — ZOUT_P = 1 when Z+ aggregated photocurrent is greater than Z- aggregated photocurrent, regardless of quadrature-track output condition **01**: Gated by A — ZOUT_P = 1 beginning at the first AOUT_P_DIG falling edge after Z+ aggregated photocurrent becomes greater than Z- aggregated photocurrent and ending at the next subsequent AOUT_P_DIG rising edge **10**: Gated by B — ZOUT_P = 1 beginning at the first BOUT_P_DIG falling edge after Z+ aggregated photocurrent becomes greater than Z- aggregated photocurrent and ending at the next subsequent BOUT_P_DIG rising edge **11**: by A & B — ZOUT_P = 1 beginning at the first AOUT_P_DIG falling edge when BOUT_P_DIG = 0 or the first falling BOUT_P_DIG falling edge when AOUT_P_DIG = 0 after Z+ aggregated photocurrent becomes greater than Z- aggregated photocurrent and ending at the next subsequent AOUT_P_DIG or BOUT_P_DIG rising edge
SE_DZ	Single-ended/differential output control: **0**: Differential — Device drives ZOUT_P, ZOUT_N to complementary logic levels **1**: Single-ended — Device places ZOUT_N in high-impedance state and only drives ZOUT_P
TLNM	Always set to ‘b1: ~~1: Low-Noise – Quad-track signal path has 3dB corner frequency limited to 400KHz~~
RSVD	Reserved for future use

The figures below depict ideal index-track output responses for a variety of combinations of code-wheel rotation direction, gating, and interpolation settings.

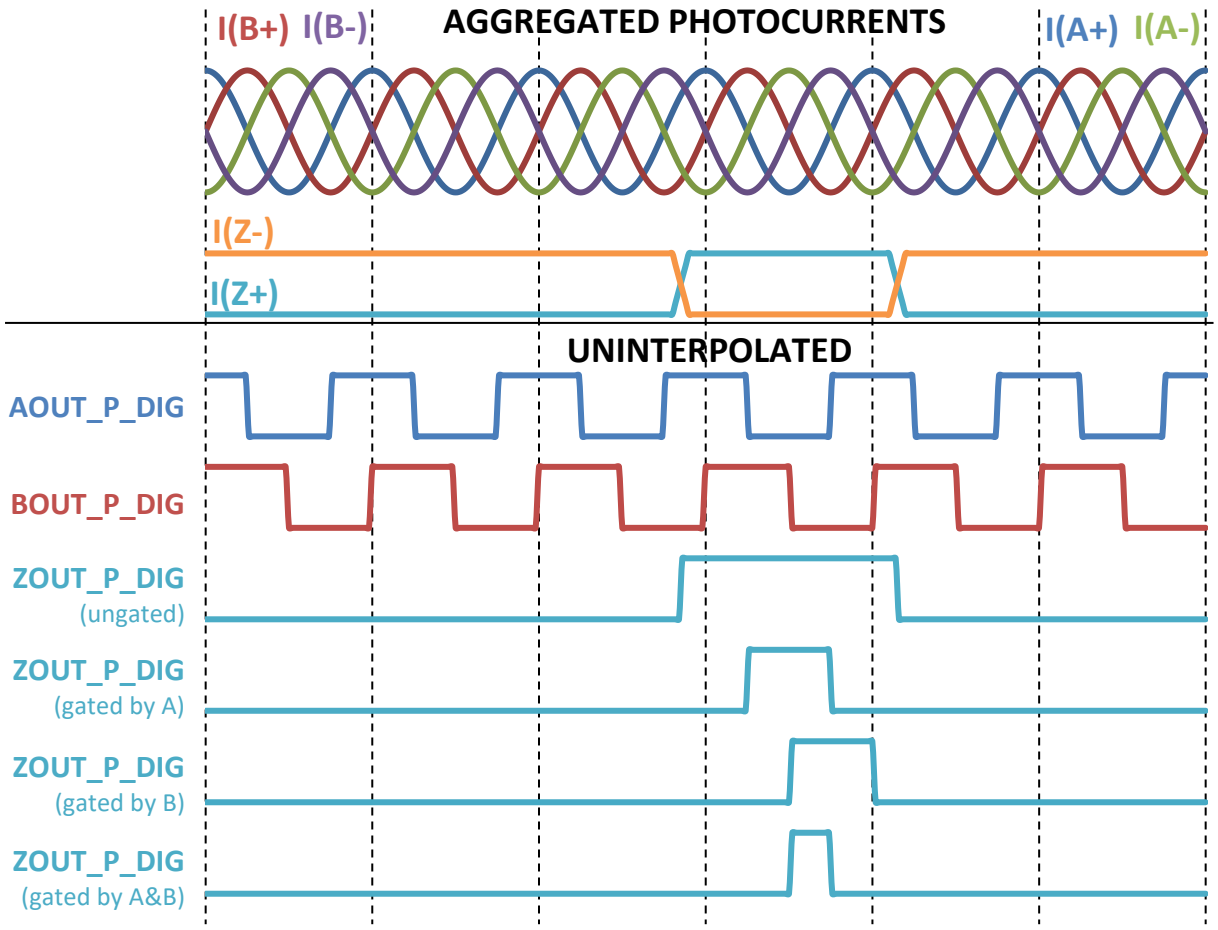

Figure 7: Index-Track Output Response (A leading B, digital, uninterpolated)

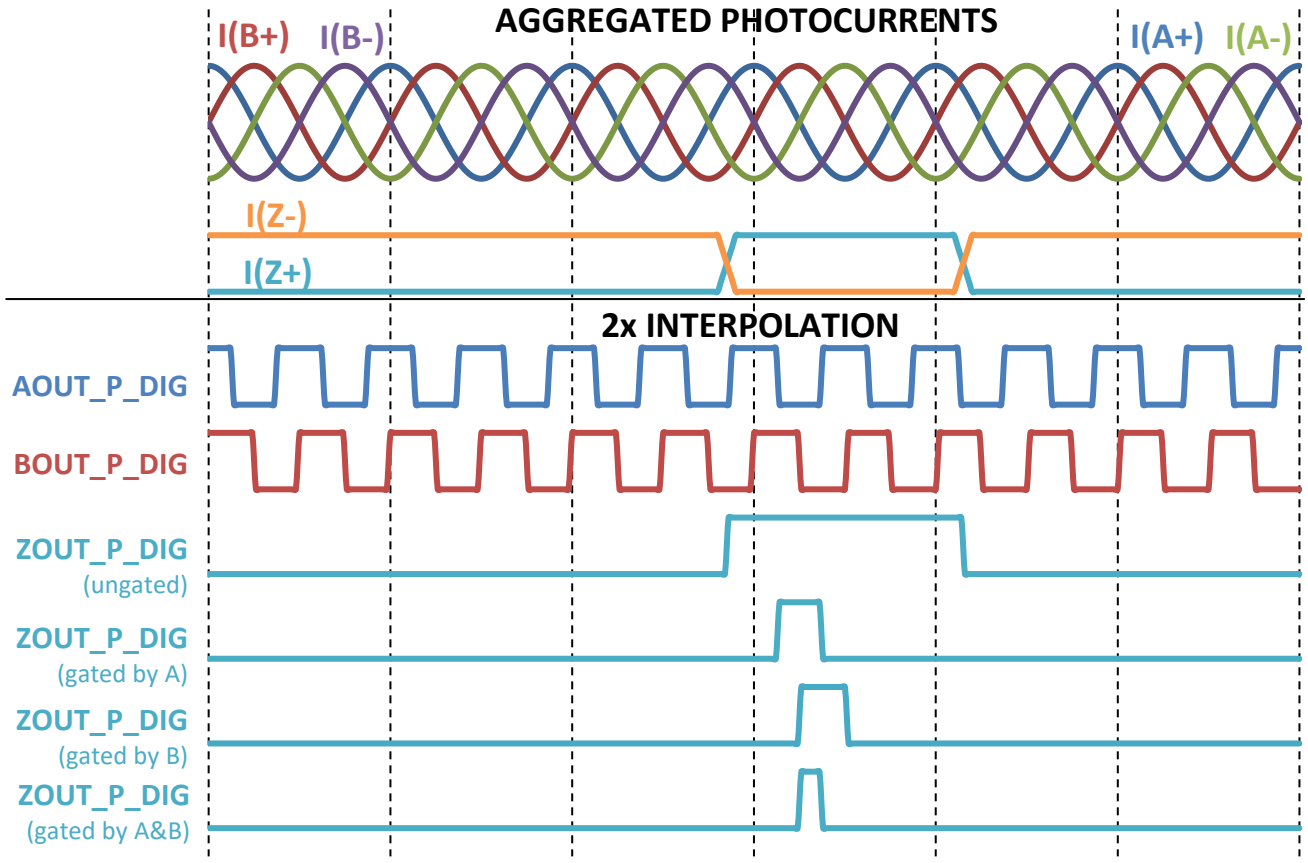

Figure 8: Index-Track Output Response (A leading B, digital, 2x interpolation)

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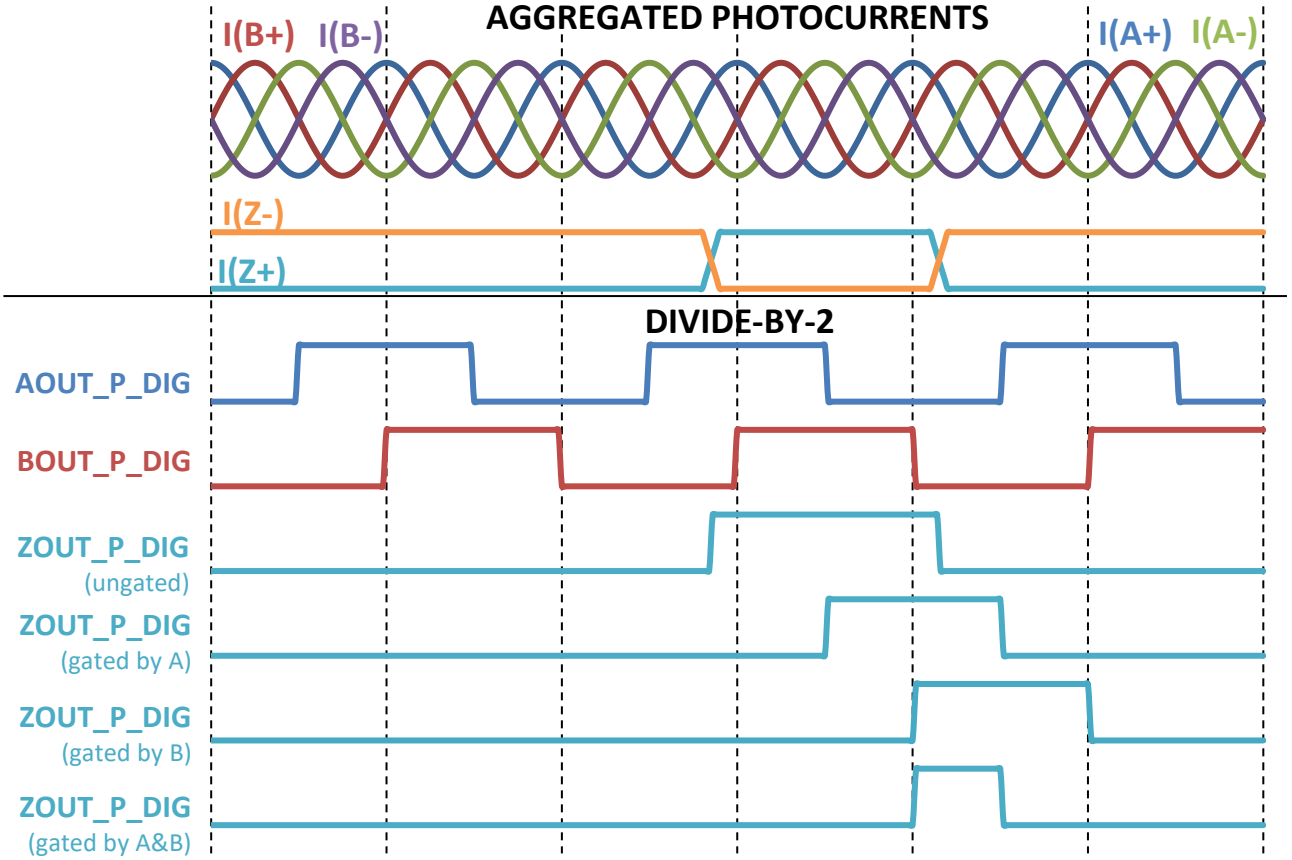

Figure 9: Index-Track Output Response (A leading B, digital, divide-by-2)

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Signal Conditioning

For ideal system-level determination of position and velocity, the sinusoidal quadrature-track analog voltages produced from the aggregated photocurrents from the FS210/FS310's properly-configured pixel array should have zero DC offset and equal amplitudes and be exactly 90° out of phase. Deviations from these ideal signal characteristics can arise from several sources, such as:

- Mismatch between the LED's emission pattern, the code wheel, and the PXC/CCFG pattern
- Imperfections in code-wheel printing
- Code-wheel eccentricity and/or presence of an out-of-plane component of rotation
- Transistor-level mismatches in the FlexSense™ chip

The FS210/FS310 contains registers to trim the quadrature-track DC offsets and amplitudes. below illustrates the quadrature-track signal path. The nominal value of the TIA feedback resistors is 230kΩ if the TLNM bit in the ZCFG control register is 0, or 700kΩ if the TLNM bit is 1. The power-on default voltage gain of the second-stage buffer is 4.

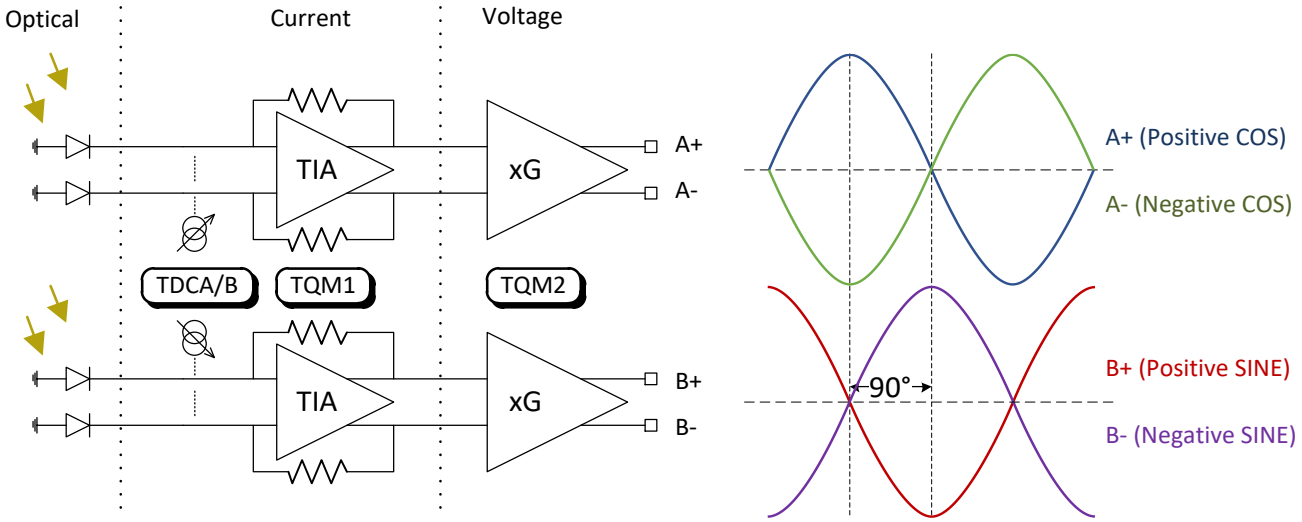

Figure 10: Differential Photocurrents (A+/A- & B+/B-) Signal paths

A small current can be injected in parallel with either the A+ or the A- aggregated photocurrent, and another small current can be injected in parallel with either the B+ or the B- aggregated photocurrent. The TDCA and TDCB trim registers, respectively, control these currents. Adding trim current in parallel with the A+ (B+) aggregated photocurrent acts to make the DC offset of the A (B) differential output voltage more positive or less negative. Adding trim current in parallel with the A- (B-) aggregated photocurrent acts to make the DC offset of the A(B) differential output voltage less positive or more negative. Up to 31 steps of 4nA each can be added to either the A+ or the A- aggregated photocurrent, and up to 31 steps of 4nA each can be added to either the B+ or the B- aggregated photocurrent.

Mismatches in the amplitudes of the A+/A- and B+/B- differential output voltages can be counteracted by reducing the feedback transresistances around whichever of the A or B transimpedance amplifier produces a greater untrimmed differential sinusoidal voltage amplitude. The TQM1 trim register controls this transimpedance attenuation: one bit selects either the A or B transresistances to be attenuated, and the remainder of the register allows the selected transresistances to be reduced by up to 7 steps of 5% each.

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Finally, the voltage gain of the second-stage buffers in both the A and B paths can be changed under the control of the TQM2 trim register. The buffer gain can be set to 4 (power-up default), 6, 8, 12, 16, 24, 32, 48 or 64. Changing the TQM2 setting changes the gains of both the A+/A- buffer and the B+/B- buffer together.

Offset Trim Register A (TDCA: [0x0880])

Table 14. TDCA register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD		SDCA	MDCA				

Table 15. TDCA field description

Bits	Description
MDCA	Magnitude: 4nA/LSB added to A+/A- transimpedance amplifier input selected by SDCA bit
SDCA	Sign bit: Selects whether extra current is to be added to positive- or negative-sense aggregated photocurrent input to A+/A- transimpedance amplifier **0**: Add current to A- aggregated photocurrent **1**: Add current to A+ aggregated photocurrent
RSVD	Reserved for future use

Offset Trim Register B (TDCB: [0x0881])

Table 16. TDCB register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD		SDCB	MDCB				

Table 17. TDCB field description

Bits	Description
MDCB	Magnitude: 4nA/LSB added to B+/B- transimpedance amplifier input selected by SDCA bit
SDCB	Sign bit: Selects whether extra current is to be added to positive- or negative-sense aggregated photocurrent input to B+/B- transimpedance amplifier **0**: Add current to B- aggregated photocurrent **1**: Add current to B+ aggregated photocurrent
RSVD	Reserved for future use

Magnitude Trim Register 1 (TQM1: [0x0882])

Table 18. TQM1 register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD				SQM1	MQM1		

Table 19. TQM1 field description

Bits	Description
MQM1	Magnitude: Feedback transimpedance resistance around selected TIA reduced by 5%/LSB
SQM1	Select bit: Selects the TIA whose feedback transresistances should be reduced **0**: Reduce B+/B- feedback transresistance **1**: Reduce A+/A- feedback transresistance
RSVD	Reserved for future use

Magnitude Trim Register 2 (TQM2: [0x0883])

Table 20. TQM2 register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD				MQM2			

Table 21. TQM2 field description

Bits	Description		
MQM2	Magnitude: Identically sets A+/A- and B+/B- buffer gains		
	0000: Gain = 4	**0011:** Gain = 12	**0110:** Gain = 32
	0001: Gain = 6	**0100:** Gain = 16	**0111:** Gain = 48
	0010: Gain = 8	**0101:** Gain = 24	**1xxx:** Gain = 64
RSVD	Reserved for future use		

LED Drive Control

The LEDK pin of the FS210/FS310 is intended to be connected to the cathode of the LED acting as the light source for the encoder system. The LED is external for the FS210 and is in-package for the FS310. The LED drive can be regulated either at a fixed current level or in a closed control loop, as selected by bit 7 of the ILED control register. The drive current can be disabled completely by writing the ILED control register to 0x00.

In a transmissive-mode design the LED is placed on the opposite side of the code wheel from the PCB containing all the other components in the encoder module, with the LEDK pin of the FlexSense™ device connected off-board to the cathode of the LED. The OP207CL IR LED from TT Electronics is recommended for use with the FS210.

In open-loop control, the current sunk by the LEDK pin is kept first-order constant at the level coded by the least-significant 7 bits of the ILED control register. ILED<6:0> is taken to represent an unsigned binary-weighted integer in the range [0, 127], and the drive current is fixed at 0.6mA/LSB nominally. Therefore, the optical power density incident to the FS210/FS310 varies directly with the LED optical output power at this fixed drive current – both with temperature (LED optical output power at a given drive current decreases with increasing temperature and vice-versa) and with LED degradation (LED optical output power at a given drive current at constant temperature decreases slowly over the operating lifetime of the LED).

In closed-loop control, the current sunk by the LEDK pin is varied in order to maintain nearly constant quadrature-track signal voltage amplitude at all operating conditions – i.e. to compensate automatically for the degradation of LED output optical power over operating life and for the heavy negative temperature dependence of LED output optical power at a given drive current – without requiring any explicit user action. At the onset of closed-loop control, the LEDK drive current is initialized to 7/8 (0.875) of the value encoded by ILED<6:0>. The LEDK drive current is decreased by 0.6mA if the quadrature-track differential output voltage amplitude is greater than the level encoded by the LEDLP control register, and the LED drive current is increased by 0.6mA if the quadrature-track differential output voltage amplitude is less than the level encoded by LEDLP and the drive current does not exceed the level encoded by ILED<6:0>. In no case can the LEDK drive current be greater than the level encoded by ILED<6:0>. The LEDK drive current is updated approximately either once every sixteen seconds or once every second, depending on the state of the FAST bit of the LEDLP control register. The value of the actual LEDK drive current can be read back through the LEDLV status register.

In closed-loop control, if the actual LEDK drive current is greater than 7/8 of the level encoded by ILED<6:0>, an alarm condition is present: bit 6 of the interrupt mask/status register is set, and an interrupt is generated if not masked by bit 2 of the interrupt mask/status register.

LED Drive Current Control Register (ILED: [0x0886])

Table 22. ILED register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
C_OZ	ILK						

Table 23. ILED field description

Bits	Description
ILK	Binary-weighted LEDK drive current (actual if C_OZ = 0, maximum if C_OZ = 'b1); 0.6mA/LSB nominally
C_OZ	Open/Closed loop current control bit: **0** Open-loop; current determined exclusively by ILK **1** Closed-loop; current set to make quad-track analog voltage conform to settings of LEDLP register if possible, without exceeding level encoded by ILK

LED Closed-Loop Control Register (LEDLP: [0x0887])

Table 24. LEDLP register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
FAST ('b0)	FB_SEL		LO_SEL		HI_SEL		

Table 25. LEDLP field description

Bits	Description
HI_SEL	Sets quadrature-track differential analog voltage amplitude; level ≈ 500mV + 100mV/LSB
LO_SEL	Should be left at power-up default 00
FB_SEL	Closed-loop control is optimized when encoded level matches factory-trimmed $V_{O:Q}$ level; **should be set to 10** **00**: 1.15V **01**: 1.20V **10**: 1.25V **11**: 1.30V
FAST	Open/Closed loop current control bit, always set to 'b0: **0** Normal update rate; drive current updated approximately once per 16 seconds

LED Drive Current Readout Register (LEDLV: [0x088F])

Table 26. LEDLV register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
C_OZR	ILKR						

Table 27. LEDLV field description

Bits	Description
ILKR	Actual LEDK drive current; 0.6mA/LSB nominally; equal to ILK if C_OZ = 0
C_OZR	Read-only duplicate of C_OZ bit in ILED register

Alarm Control

- Four types of events cause the FS210/FS310 to register an alarm condition when detected:
  - Power-up sequence initiated. (Alarm condition ends when power-up sequence is complete.)
  - Control loop out of regulation for closed-loop LED-drive control. (Alarm condition ends when control loop re-enters regulation.)
  - On-chip junction temperature exceeds a user-configurable alarm trip point. (Alarm condition ends when junction temperature falls below thermal-alarm trip point.)
  - On-chip junction temperature exceeds approximately 165°C, at which point the device might suffer damage. (Power-cycling required to terminate alarm condition, even if junction temperature falls below 165°C.)
- The presence of an alarm condition causes the corresponding status bit in the INTR register to be set to 1. The status bit is cleared to 0 only upon an I^2C read access to INTR or upon a power-on reset. The disappearance of the alarm condition alone, without such an I^2C read access or POR event, is insufficient to clear an interrupt status bit to 0. Additionally, the presence of a (Tj > 165°C) alarm condition, because it suggests excessive power dissipation, causes all current-consuming circuitry in the device to be shut off. Accordingly, this alarm condition is termed a thermal-shutdown alarm condition.
- Unmasked alarm conditions cause the device's open-drain IRQZ pin to be driven low; masked alarm conditions cause no activity on the IRQZ pin. Power-on-sequence alarm conditions are unmaskable and therefore always cause IRQZ to be driven low. The other three alarm conditions are masked (and therefore cause no IRQZ activity) if the corresponding mask bit in the INTR register is cleared to 0 and unmasked (and therefore do cause IRQZ activity) if the corresponding mask bit in INTR is set to 1. IRQZ is driven low only for as long as an unmasked alarm condition persists: the termination of an unmasked alarm condition causes the device to release the IRQZ pin, even though the corresponding INTR status bit stays set to 1 until an I^2C read access or POR event.

Thermal Alarm Register (TALM: [0x0888])

Table 28. TALM register definition.

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
TTRM				TASET			

Table 29. TALM field description.

Bits	Description
TASET	Thermal alarm trip point encoding: Trip point (T_{jAL}) = 200°C – 9°/LSB
TTRM	Thermal accuracy trim *(An I^2C write access to TALM to change TASET should be preceded by an I^2C read access to ascertain the state of TTRM so that the I^2C write access does not change TTRM.)*

Interrupt Mask/Status Register (INTR: [0x0889])

Table 30. INTR register definition.

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
ISPS	ISLC	ISTA	ISTS	RESV	IMLC	IMTA	IMTS

Table 31. INTR field description.

Bits	Description
IMTS	Interrupt mask bits for thermal shutdown condition: **0**: Thermal shutdown condition does not cause IRQZ = 0 **1**: Thermal shutdown condition does cause IRQZ = 0
IMTA	Interrupt mask bit for thermal alarm condition: **0**: Thermal alarm condition does not cause IRQZ = 0 **1**: Thermal alarm condition does cause IRQZ = 0
IMLC	Interrupt mask bit for LED control loop out-of-regulation: **0**: LED control loop out-of-regulation condition does not cause IRQZ = 0 **1**: LED control loop out-of-regulation condition does cause IRQZ = 0
RSRV	Reserved for future use
ISTS	Read-only interrupt status bit for thermal shutdown condition: → **1** if on-chip junction temperature exceeds 165°C
ISTA	Read-only interrupt status bit for thermal alarm condition: → **1** if on-chip junction temperature exceeds value encoded by TASET
ISLC	Read-only interrupt status bit for LED control loop out-of-regulation: → **1** if actual LED drive current exceeds 7/8 of the value encoded by ILED<6:0>
ISPS	Read-only interrupt status bit for power-up sequence: → **1** when VDD/VDDA voltage rises above power-on reset trip point

Other Registers

The FS210/FS310 contains two registers that selectively power down portions of the quadrature-track and index-track signal-path circuitry: the Transimpedance Amplifier Enable (TIAE) and Comparator/Buffer Enable Register (CBFEZ) registers. There are two situations in which it might be desirable to modify the contents of these registers from their power-on defaults in order to reduce the supply current consumed by the device:

- If the device is deployed in a system whose code wheel does not contain an index track, then TIAE and CBFEZ can be modified to turn off the index-track transimpedance amplifier and comparator.
- If the device is in a system in which QCFG is configured only for analog outputs and/or uninterpolated digital outputs, then CBFEZ can be modified to turn off the interpolated quad-track comparators.

In all other cases, the contents of TIAE and CBFEZ should not be modified from their power-on defaults.

The FS210/FS310 also contains a Miscellaneous Control Register (MISC), which can be used to enable the preventive-maintenance outputs on the IPTAT, AMPL2_P, and AMPL2_N pins. If these outputs are enabled, the IPTAT pin sinks a current that is first-order proportional to absolute temperature and is nominally equal to 10µA at 25°C, and the AMPL2_P and AMPL2_N pins source currents whose difference is the sum of the squares of the analog quadrature-track differential output voltages (which should be constant if the device is configured properly and the system has no mechanical-integrity issues).

Transimpedance Amplifier Enable Register (TIAE: [0x088A])

Table 32. TIAE register definition

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD					ZTIAE	RSVD	

Table 33. TIAE field description

Bits	Description
ZTIAE	Index-track transimpedance-amplifier enable bit: **1**: Enable index-track transimpedance amplifier (power-on default) **0**: Disable index-track transimpedance amplifier
RSVD	Reserved; do not modify from power-on default value (1)

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Comparator/Buffer Enable Register (CBFEZ: [0x088B])

Table 34. CBFEZ register definition.

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD					ZCEZ	QICEZ	RSVD

Table 35. CBFEZ field description.

Bits	Description
QICEZ	Quad-track interpolated comparator enable bit: **0**: Enable quad-track comparators required to produce interpolated outputs (power-on default) **1**: Disable quad-track comparators required to produce interpolated outputs
ZCEZ	Index-track comparator enable bit: **0**: Enable index-track comparator (power-on default) **1**: Disable index-track comparator
RSVD	Reserved; do not modify from power-on default value (0)

Miscellaneous Control Register (MISC: [0x088D])

Table 36. MISC register definition.

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
RSVD		PMOUT		RSVD			

Table 37. MISC field description.

Bits	Description
PMOUT	Preventive-maintenance output control bits: **00**: Disable preventive-maintenance outputs (power-on default) **11**: Enable preventive-maintenance outputs **01, 10**: Prohibited
RSVD	Reserved; do not modify from power-on default value (<7:6> = 00; <3:0> = 0001)

Power-Up Sequence

When the voltage on the FS210/FS310's digital and analog supply pins VDD and VDDA rises above the power-on reset trip point, a power-up sequence is initiated. The device's behavior varies depending on the logic level on the MODE pin at power-on reset. If MODE = 1, the device completes a *master-mode* power-up sequence. If MODE = 0, the device completes a *slave-mode* power-up sequence.

In both master-mode and slave-mode power-up sequences, the FS210/FS310 sets the ISPS status bit (bit 7 of the Interrupt Mask/Status Register INTR) to 1 and drives the IRQZ pin low as soon as the VDD/VDDA voltage rises above the power-on reset trip point. For the next approximately 2.5ms, the device performs an internal self-configuration routine.

In a master-mode power-up sequence, when the self-configuration routine is complete, the device, acting as an I^2C master, executes an I^2C read access to an off-chip non-volatile memory device such as the M24C32S-FCU from ST Microelectronics, wherein the contents of addresses [0x0000-0x01FF], [0x0400-0x041F], and [0x0880-0x088C] in the off-chip memory device are copied into the same addresses in the FlexSense™ device (PXC, CCFG, and miscellaneous configuration registers, respectively). If this I^2C read access is successful and if the data byte copied into the device's SIG register ([0x088C]) is equal to 0xAA, then the device sets its SIGV register ([0x088E]) to 0x0A. When the I^2C read access is complete (whether successful or not), the device releases the IRQZ pin, and the power-up sequence is complete.

In a slave-mode power-up sequence, the FS210/FS310 does not execute an I^2C read access to an off-chip non-volatile memory device, and the device releases the IRQZ pin as soon as the self-configuration routine is complete, indicating the completion of the power-up sequence. In this case, the device's PXC and CCFG registers are in random states and the rest of the configuration registers contain their power-on default values at the completion of the power-up sequence. Therefore, proper operation of the FS210/FS310 depends upon the loading of values into these registers consistent with the system in which the device is deployed, via one or more I^2C write accesses to the device from a bus master elsewhere in the system.

Throughout the duration of the power-up sequence – i.e. while the device is driving the IRQZ pin low, external I^2C write and read accesses are prohibited, and any such I^2C accesses are ignored by the device. I^2C write and read accesses are accepted by the device once the IRQZ pin is released at the end of the power-up sequence.

I^2C Interface

The I^2C interface is used to read from and write to the FS210/FS310's registers. The device functions as a fast-mode (max 400 Kbit/s) slave device (except during a master-mode power-up sequence, when it functions as a master), according to the I^2C specification document, located at:

http://www.nxp.com/documents/user_manual/UM10204.pdf

The FlexSense™ device, when in slave mode, includes all the mandatory features (START and STOP condition recognition, acknowledgement, 7-bit slave address) and none of the optional slave-device features specified by the I^2C standards. Both I^2C pins, SCL and SDA, are open-drain, and they both require off-chip external pullup resistors to VDD. The SCL pin is driven by whichever device on the I^2C bus is the bus master, and the SDA pin is driven by whichever device is transmitting a data bit.

The figure below illustrates the transfer of data bits on the I^2C bus.

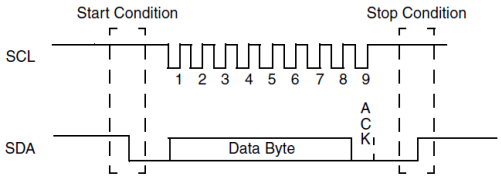

Figure 11: I²C Bit Transfer

During data transfer the logic level on SDA may be changed only when a low logic level is present on SCL. (A change in SDA logic level when SCL is high is interpreted as either a S(START) condition or a P(STOP) condition.) The "S" condition is generated by creating a falling edge on the SDA pin while the SCL pin is at a high logic level. The "P" condition is generated by creating a rising edge on the SDA pin while the SCL pin is at a high logic level. All I²C bus transactions must begin with a master-generated "S" condition. All transactions should end with a master-generated "P" condition. The FS210/FS310 will not accept a START-Repeat (Sr) condition, so all commands must have explicit Start and Stop conditions.

For data bits being transmitted to the device, the FS210/FS310 determines the bit value by sampling SDA at SCL↑. For logic-0 data bits being transmitted by the device, the FS210/FS310 begins to drive SDA low[1] immediately after SCL↓, so that the I²C master can determine the bit value of SDA at the following SCL↑.

All data bytes are transmitted MSB-first, and all data bytes include a 9th SCL period in which the device that received the byte acknowledges, either positively (A) or negatively (A\), to the device that transmitted the byte.

When the FS210/FS310 is acting as an I²C master – only during a power-up sequence when the MODE pin is at a high logic level – it is expected to read data from an off-chip non-volatile memory connected to the same I²C bus. During a master-mode power-up sequence, the device directs I²C read accesses to the off-chip non-volatile memory with a fixed device address of 0x50. Contact the factory if an off-chip non-volatile memory with a different I²C slave address is required.

When the FS210/FS310 is acting as a slave – any time not during a power-up sequence – it comprehends two I²C commands: Write To Slave and Read From Slave. Both command sequences begin with a start condition, followed by a 7-bit slave address transmitted from the I²C bus master to the FlexSense™ device:

- I²C slave address with a "Write" direction bit (SA-W).
  - The 7-bit I²C slave address assigned to the FS210/FS310 is 'h31. The direction bit is appended at the least-significant end of the 7-bit I²C slave address. A "Write" direction bit is encoded as 0, so the entire byte is 'b1100010 = 'h62.
  - Two-byte FS210/FS310 target address for the Write command, transmitted least-significant-byte-first.
  - 0 or more bytes may follow. The address pointer self-increments after every successfully written byte.
- I²C slave address with a "Read" direction bit (SA-R).
  - A "Read" direction bit is encoded as 1, so the slave address would be 'b1100011 = 'h63
  - 0 or more bytes can then be read from the FlexSense™ device starting at the last address pointer. The address pointer self-increments after every successfully read byte.
  - The master can signify that the reads are complete by issuing a NACK on the last desired byte, i.e. by not acknowledging the last byte on the ninth bit.

[1] To transmit a logic-1 data bit, the FS210 does not drive **SDA** at all – it is an open-drain pin.

The FS210/FS310 acknowledges (A) each byte successfully matched slave address and after every byte during a slave write sequence. If the slave address embedded in the SA-W byte does not match the slave address assigned to the FS210/FS310, then the device negative-acknowledges (A\) the SA-W byte and all subsequent bytes until the next detected start (S) condition.

For a Write Memory command sequence, the I²C bus master should follow the slave address immediately (with no intervening stop, start, or start-repeat condition) by a 2-byte register address (LSB first) and then a series of data bytes, each of which is acknowledged (A) by the FS210/FS310. The first such data byte is stored in the device register specified by the 2-byte target address in the preamble. Subsequent data bytes, if any, are stored at consecutively increasing register addresses. After the last data byte is transmitted, the I²C bus master should transmit a stop condition (P) to terminate the Slave Write sequence. This sequence is depicted graphically in the figure below, where elements in **black** indicate transmission from the I²C bus master to the device and elements in **blue** indicate transmission from the device to the I²C bus master.

Figure 12: Write Memory Command Sequence

For a Read Memory command sequence, the I²C bus master should issue a slave write followed by the 2-byte register address, a Stop (S) condition, then a "Slave Address – Read" (SA-R) byte (assigned 7-bit I²C slave address a "Read" direction bit appended at the least-significant end, or 'h63), which the FS210/FS310 acknowledges (A), provided the 7-bit slave address embedded in the SA-R byte matches that assigned to the device (0110001b) and which it negative-acknowledges (A\) otherwise. Following the SA-R byte, the device transmits a series of data bytes, of which the first is the contents of the register at the target address specified in the 3-byte preamble and of which subsequent bytes, if any, are the contents of registers at consecutively increasing addresses. The I²C bus master should acknowledge (A) a data byte if it is not the last data byte intended to be read, and it should negative-acknowledge (A\) the last data byte it intends to read. After such a negative-acknowledgement from the I²C bus master, the device ignores all I²C traffic until the next start or start-repeat condition is issued.

CAUTION: The I²C Repeated Start (Sr) command is not implemented on the FS210/FS310. Any usage of the Repeated Start will give undefined behavior.

Figure 13: Read Memory Command Sequence

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Typical Application Circuit

A schematic representation of a typical application circuit is shown below, one each for the FS210 and FS310. In this circuit, the device is configured for master-mode power-up sequences: the MODE pin is pulled high, and a M24C32 non-volatile EEPROM device is placed on the same I^2C bus. This circuit would be most appropriate for a system design in which there is no microcontroller with an I^2C port in the system to store configuration data and load them into the device upon power-up in the field. If such a microcontroller is available in the system, the MODE pin of the device would be pulled low, the M24C32 device would be absent, and the I^2C bus lines (SCL, SDA) would be brought out to connect to the I^2C port of the microcontroller. The typical application circuit contains a visible LED in series with a current-limiting resistor connected to the open-drain IRQZ pin of the device to produce a visible indication of an alarm condition.

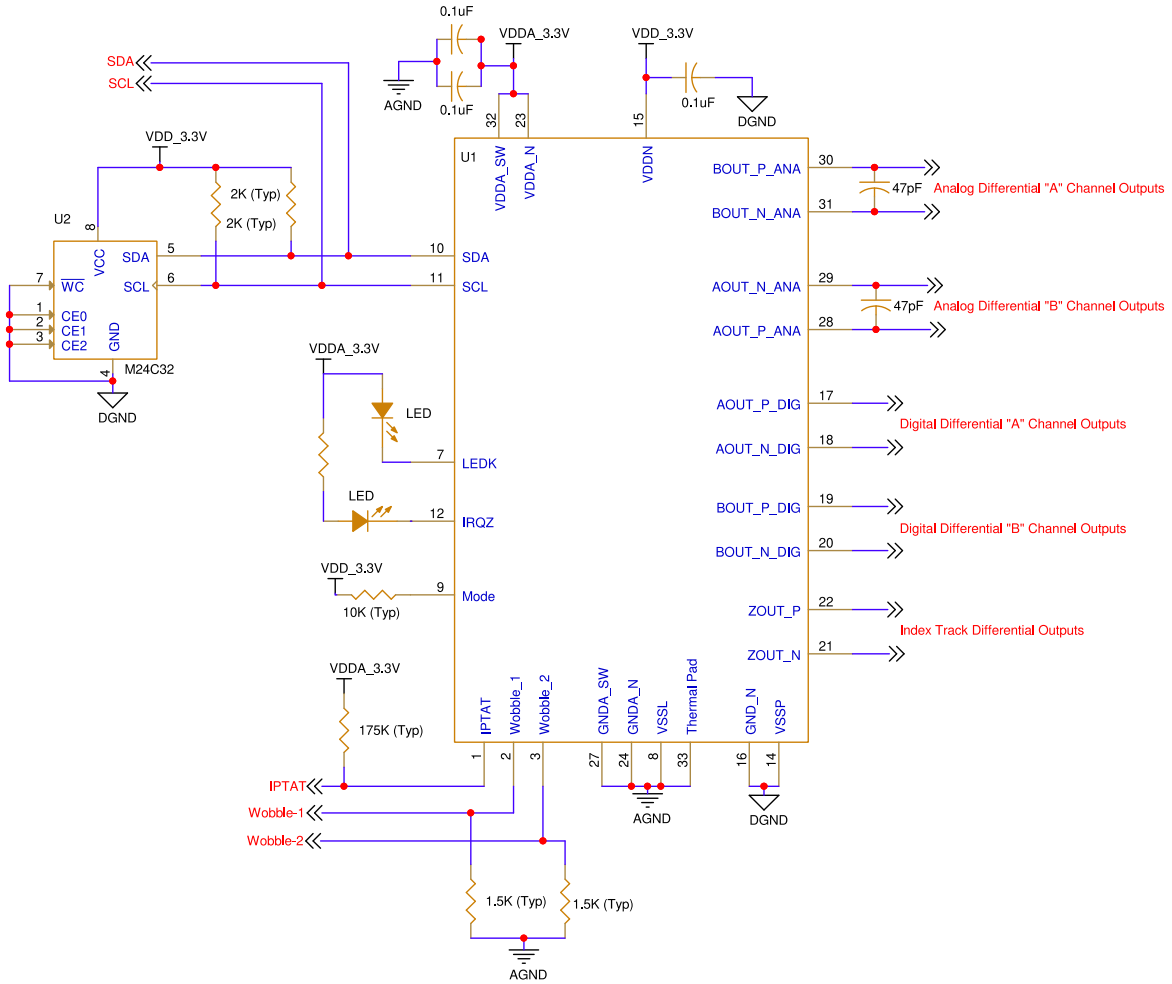

Figure 14: FS210 Typical Application Circuit

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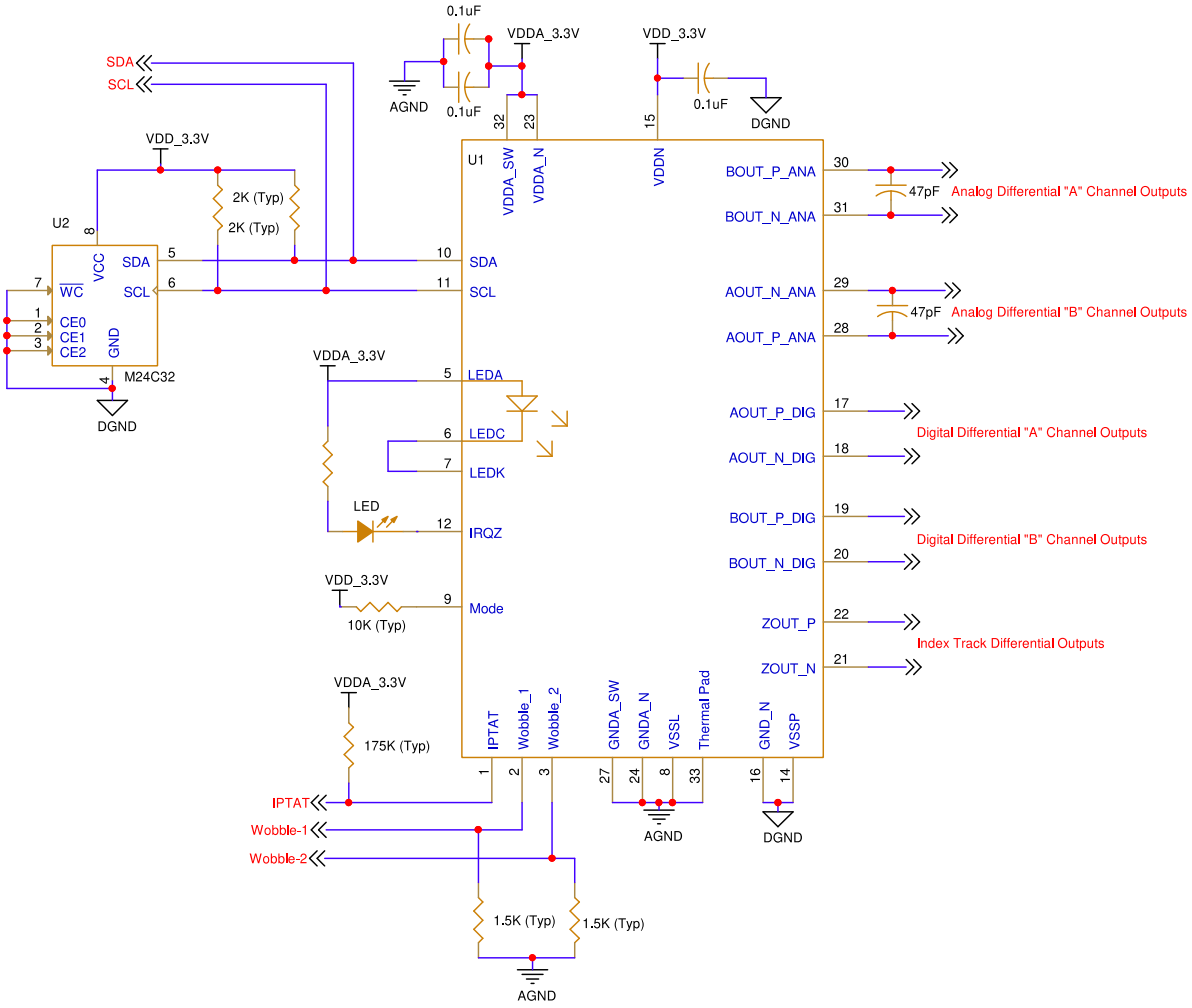

Figure 15: FS310 Typical Application Circuit

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Package Information

5x5x0.65mm / 0.50mm Pitch / 32L
FS210/310 Package Outline Drawing

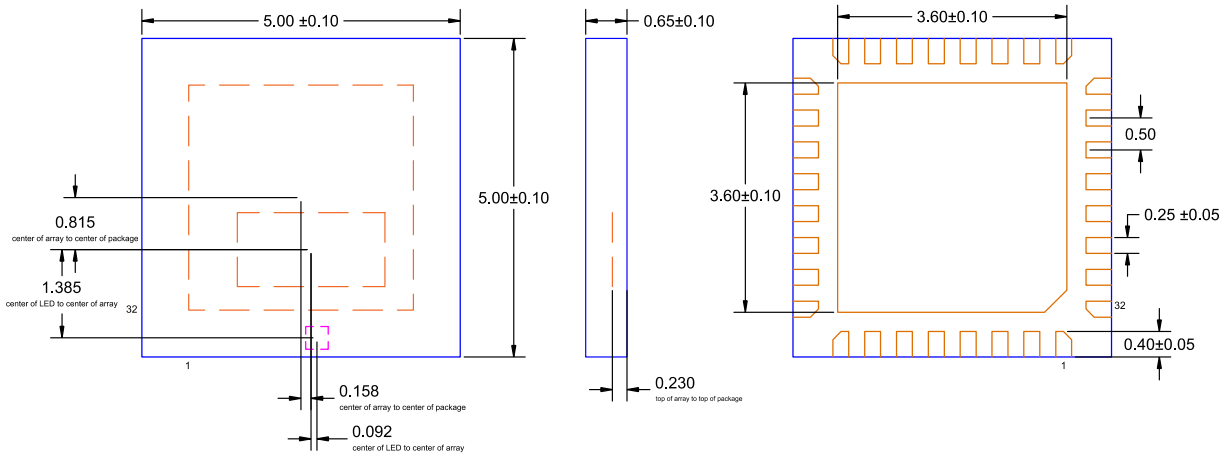
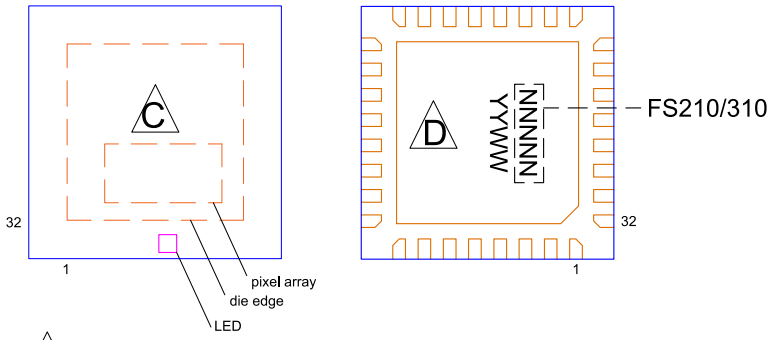


Figure 16: Package Outline Drawing. Only the FS310 has the LED in the QFN package. All other dimensions are identical.

5x5x0.65mm / 0.50mm Pitch / 32L
FS210/310 Package Branding



C - Die Side
- Clear mold compound laser marking is not recommended.

D - IO Pad Side
- Standard branding reference
  N - Product part number
  Y - Last two digit of year of manufacture
  W - Week of manufacture

Backside laser marking only.
No ink marking allowed.

Figure 17: Brand Specification. Only the FS310 has the LED in the QFN package.

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Recommended Reflow Profile

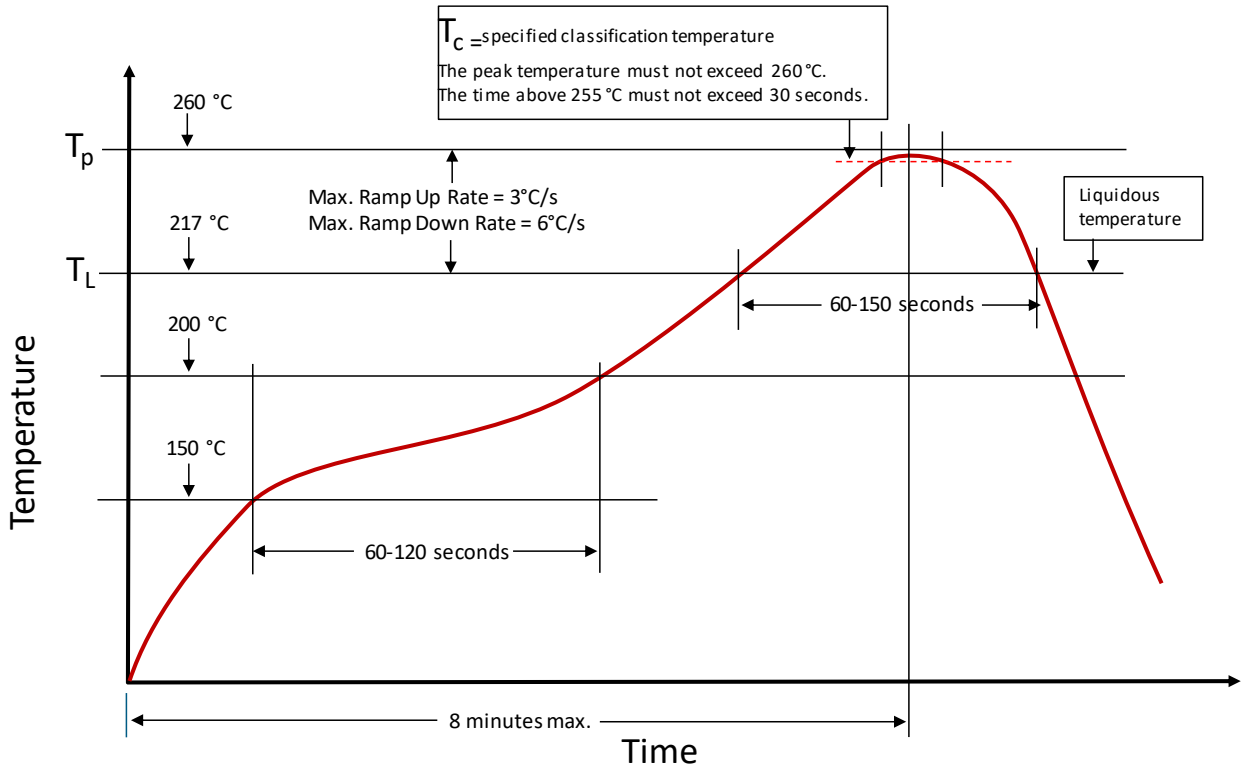

Figure 18. Recommended reflow profile at MSL-6 rating.

Shelf Life

All parts are shipped in Moisture Barrier Bags with desiccant to protect them against ambient moisture in the environment. The parts can be stored in their original, unopened bags for 12 months at < 40°C, < 90% RH, after which, their shelf life will have been exceeded.

Floor Life

The FS210 and FS310 parts have been qualified for Moisture Sensitivity Level 6. Once the Moisture Barrier Bags have been opened in an ≤ 30°C/60% RH manufacturing environment, the parts must be soldered within 8 hours, after which, their floor life will have been exceeded.

Rebaking Instructions

All parts that exceed the shelf life or floor life must be rebaked using one of the following options:

- 125°C for 4 hours, < 5% RH
- 85°C for 18 hours, < 5% RH

List of Figures

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